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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/937,680	11/29/2001	Zahid Ansari	19730-000110US	3828

20350 7590 05/09/2003

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/937,680	ANSARI ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26-30* is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *21-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11/29/01 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 6-8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 7-9, 11-15 and 21-25 are objected to because of the following informalities:

Claims 7-9 are objected because the citation "operable", in line 2 of each claim, is not a positive citation.

Claims 11-14, 21 and 24 are objected with similar reasons.

Claims 15, 22, 23 and 25 are objected as including the informalities of one of the claims above.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa et al. (USP 5021936).

As to claim 1, Nishuzawa et al. discloses in figures 1 and 3 a method comprising: providing a DC voltage signal (15); utilizing a first switching circuit (11, 12) to switch the DC

voltage signal so as to produce relative to a reference voltage a positive pulse width modulated voltage signal for about one half of a fundamental output period (shown in figure 3G and 3H); utilizing a second switching circuit (13, 14) to switch the DC voltage signal so as to produce relative to the reference voltage a negative pulse width modulated voltage signal for about one half of the fundamental output period (shown in figure 3G and 3H) (figure 3 shows all of the switch circuits are used in the first haft and second haft of the fundamental output period).

As to claim 2, figures 1 and 3 show the step of reversing the polarity of the DC voltage signal after switching the DC voltage signal for about one half of the fundamental output period (in the first haft of the fundamental output period, the output signal having positive polarity, and in the second haft of the fundamental period, the output signal having negative polarity).

As to claim 3, figures 1 and 3 show the step of utilizing the first switching circuit (11 and 12) to reverse the polarity of the DC voltage signal (the first switching circuit (11 and 12) have to be used along with the second switching circuit in the second haft period in order to reverse the polarity of the DC voltage signal).

As to claim 4, figures 1 and 3 show the step of utilizing the second switching circuit (13 and 14) to reverse the polarity of said DC voltage signal (the second switching circuit (13 and 14) have to be used along with the first switching circuit in the second haft period in order to reverse the polarity of the DC voltage signal).

As to claim 5, figures 1 and 3 show the step of utilizing a two switch network (11 and 12) as the first switching circuit; electrically coupling the two switch network in parallel with the DC voltage signal; utilizing a two switch network (13 and 14) as the second switching circuit; electrically coupling the two switch network of the second switching circuit in parallel with the

DC voltage signal; configuring an output (signal, shown in figure 3G), between the input terminal of circuit 16) between the two switch network of the first switching circuit and the two switch network of the second switching circuit.

As to claim 6, figures 1 and 3 show an apparatus comprising: an input (terminals that receiving 15) to receive a DC voltage signal (15); a first switching circuit (11 and 12) configured to modulate the DC voltage signal so as to produce relative to a reference voltage a positive pulse width modulated voltage signal for about one half of a fundamental output period; a second switching circuit (13 and 14) configured to modulate said DC voltage signal so as to produce relative to the reference signal a negative pulse width modulated voltage signal for about one half of the fundamental output period (figure 3).

As to claim 7, figures 1 and 3 show a circuit (circuit, not shown, that generating signals 3C-3F in figure 3 and circuits 11-14) operable to reverse the polarity of the DC voltage signal (the polarity of the output of circuit figure 1 is determined by the inputs of the switch circuits).

As to claim 8, figures 1 and 3 show the first switching circuit (104) is operable to reverse the polarity of said DC voltage signal (in order to reverse the polarity of the DC signal in the second haft period, circuit (11, 12) have to be used along with circuit (13 and 14)).

As to claim 9, figures 1 and 3 show the second switching circuit (13 and 14) is operable to reverse the polarity of said DC voltage signal (in order to reverse the polarity of the DC signal in the second haft period, circuit (13 and 14) have to be used along with circuit (11 and 12)).

As to claim 10, figures 1 and 3 show the first switching circuit comprises a two switch network (11 and 12) in parallel with the DC voltage signal and wherein the second switching circuit comprises a two switch network (13 and 14) in parallel with the DC voltage signal; and

further comprising an output (input terminals of circuit 16 in figure 1) electrically coupled between the two switch network of the first switching circuit and the two switch network of the second switching circuit.

As to claim 11, figures 1 and 3 show an apparatus for providing a pulse width modulated voltage signal, the apparatus comprising: an input (nodes that receiving 15) to receive a DC voltage signal (15); a first switching circuit (11 and 12) electrically coupled to the input so as to be electrically coupled to the DC voltage signal during operation; a second switching circuit (13 and 14) electrically coupled to the input so as to be electrically coupled to the DC voltage signal during operation; wherein the first switching circuit (11 and 12) is operable to produce a positive pulse width modulated output signal relative to a reference voltage; and wherein the first switching circuit (11 and 12) is operable to reverse the polarity of said DC voltage signal applied to a load during operation (all two of the switch circuits are used in the first haft of the fundamental period and second haft period of the fundamental period).

As to claim 12, figures 1 and 3 show the second switching circuit (13 and 14) is operable to produce a negative pulse width modulated output signal relative to the reference voltage (all two of the switch circuit are used in the first haft of the fundamental period and second haft period of the fundamental period).

As to claim 13, figures 1 and 3 show the second switching circuit (204) is operable to reverse the polarity of said DC voltage signal (all two of the switch circuit are used in the first haft of the fundamental period and second haft period of the fundamental period).

As to claim 14, figures 1 and 3 show the first switching circuit comprises a first switch (11) and a second switch (12), the first switch and second switch operable to reverse the polarity

of the DC voltage signal when the first switch is placed in a conducting state and the second switch is placed in a non-conducting state (column 5, lines 45-53, teaches that switch elements 11 to 14 are controlled in accordance with the bridge-switching signal shown in FIGS. 3C and 3D and the PWM signals shown in FIGS. 3E and 3F. It is understood that the input terminals of circuits 11-14 are respectively coupled to signals 3C-3F. Figures 3 shows the polarity of the DC voltage signal is reversed when signal 3C is high (circuit 11 is in conduct state) and signal 3D is low (circuit 12 is in non-conduct state)).

As to claim 15, figures 1 and 3 show the input is electrically coupled in parallel with the first switching circuit and the second switching circuit.

As to claim 16, figures 1 and 3 show a method of providing a pulse width modulated output voltage signal, said method comprising: providing a DC voltage signal (15); providing a first switching circuit (11 and 12) electrically coupled to the DC voltage signal; providing a second switching circuit (13 and 14) electrically coupled to the DC voltage signal; operating the first switching circuit to produce a positive pulse width modulated output signal relative to a reference voltage; operating first switching circuit to reverse the polarity of the positive pulse width modulated output signal once during a fundamental output period (the states of the switch 11 and switch 12 are changed in order to reverse the polarity of the DC signal).

As to claim 17, figures 1 and 3 show the step of operating the second switching circuit to produce a negative pulse width modulated output signal relative to the reference voltage (switches 13 and 14 operating continuously operating during a second haft of the fundamental output period).

As to claim 18, figures 1 and 3 show the step of operating the second switching circuit (13 and 14) to reverse the polarity of said output signal (at the end of the period, the polarity of the output signal is reverse back to positive).

As to claim 19, figures 1 and 3 show first switching circuit (11 and 12) comprises a first switch (12) and a second switch (11), and shows the step of reversing the polarity of positive pulse width modulated output signal by maintaining the first switch in a non-conducting state (signal D in figure 3 is low, therefore switch 12 is off) while maintaining the second switch in a conducting state (signal C in figure 3 is high, therefore switch 11 is on).

As to claim 20, figures 1 and 3 show the step of electrically coupling the DC voltage signal in parallel with the first switching circuit; and electrically coupling the DC voltage signal in parallel with said second switching circuit.

Allowable Subject Matter

Claims 21-25 would be allowable if rewritten to overcome the objection above.

Claims 26-30 are allowed.

Claims 21-25 would be and claims 26-30 are allowable because the prior art fails to teach or suggest an apparatus of claim 21 and the method of claim 26 in which the switches are operated to produce a first polarity output signal by switching the first and second switches of the first switching circuit at a modulation frequency, while the third and fourth switches of the second switching circuit are respectively held in a conducting and non-conducting condition. And, the switches are operated to produce a second polarity output signal by holding the first and second switches non-conducting and conducting condition, while the third and fourth switches are switched at the modulated frequency.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
May 5, 2003

Quan Tra
Art 2816